CLAIMS

What is claimed is:

1. A method of fabricating a capacitor in a semiconductor substrate, comprising:

forming a trench having side walls and a bottom surface in the semiconductor substrate;

forming a first layer within the trench;

removing the first layer from the bottom surface of the trench;

forming a first conductive layer on the trench;

recessing the first conductive layer within the trench;

removing the first layer from the side walls of the trench, forming a structure protruding from the bottom surface of the trench;

depositing a doped insulating layer on the trench;

driving out charged elements from the doped insulating layer into the semiconductor substrate, forming a doped substrate region;

removing the doped insulating layer from the trench forming a first electrode;

forming a dielectric layer within the trench;

forming a second conductive layer on the trench, and

recessing the second conductive layer within the trench forming a second electrode.

2. The method according to claim 1, wherein the semiconductor substrate is silicon or germanium.

3. The method according to claim 1, wherein before forming the trench in the semiconductor substrate, a first masking layer is formed on the semiconductor substrate.

4. The method according to claim 1, wherein the first layer is an oxide layer.

5. The method according to claim 1, wherein the first layer is removed from an upper surface of the semiconductor substrate, and from the bottom surface of the trench by a spacer etch process.

6. The method according to claim 1, wherein the first conductive layer is a polycrystalline silicon layer.

7. The method according to claim 1, wherein the doped insulating layer is arsenic-silicate glass (ASG).

8. The method according to claim 1, wherein the dielectric layer is a node nitride.

9. The method according to claim 1, wherein the second conductive layer is polycrystalline silicon doped with arsenic ions or phosphorous ions.

10. A method of fabricating a trench capacitor in a semiconductor substrate, comprising:

forming a trench having sidewalls and a bottom surface in the semiconductor substrate;

forming a first layer on the side walls and the bottom surface of the trench;

removing the first layer from the bottom surface of the trench;

forming a first conductive layer on the semiconductor substrate and on the trench;

recessing the first conductive layer and the first layer a predetermined distance in the trench;

driving out charged elements from the first layer into the semiconductor substrate, to form a doped substrate region;

removing the first layer from the sidewalls of the trench forming a protrusion within the trench and a first electrode;

forming a dielectric layer on the sidewalls of the trench and on the protrusion;

forming a second conductive layer on the trench, and

removing a portion of the second conductive layer from the trench forming a second electrode.

11. The method according to claim 10, wherein the semiconductor substrate is silicon or germanium.

12. The method according to claim 10, wherein before forming the trench in the semiconductor substrate, a first masking layer is formed on the semiconductor substrate.

13. The method according to claim 10, wherein the first layer is an oxide layer.

14. The method according to claim 10, wherein the first layer is removed from the upper surface of the semiconductor substrate, and from the bottom surface of the trench by a spacer etch process.

15. The method according to claim 10, wherein the first conductive layer is a polycrystalline silicon layer.

16. The method according to claim 10, wherein the doped insulating layer is arsenic-silicate glass (ASG).

17. The method according to claim 10, wherein the dielectric layer is a node nitride.

18. The method according to claim 10, wherein the second conductive layer is polycrystalline silicon doped with arsenic ions or phosphorous ions.

19. An integrated circuit device, comprising:

a semiconductor substrate having a trench;

a protrusion extending from a bottom of said trench forming a first conductive plate;

a dielectric layer formed on the first conductive plate, and

a second conductive plate formed on the dielectric layer.

20. The device according to claim 19, wherein the semiconductor substrate is silicon or germanium.

21. The device according to claim 19, wherein the protrusion extending from the bottom of the trench is polycrystalline silicon.

22. The device according to claim 19, wherein the dielectric layer is a node nitride.

23. A method of fabricating a capacitor in a semiconductor substrate having a trench with a bottom and side walls, comprising:

forming a first layer on the walls of the trench;

forming a first conductive layer in the trench;

recessing the first conductive layer within the trench;

removing the first layer to form a conductive structure within the trench;

implanting impurities into the semiconductor substrate, in the vicinity of the conductive structure;

forming a dielectric layer on the walls of the trench and on the conductive structure; and

forming a second conductive layer on the dielectric layer.

24. A method of fabricating a capacitor in a semiconductor substrate having a trench with a bottom and side walls, comprising:

forming a doped insulator on the walls of the trench;

forming a first conductive layer in the trench;

recessing the first conductive layer and the doped insulator a predetermined distance in the trench such that a remainder portion of first conductive layer is sandwiched by the doped insulator;

driving out charge elements from the doped insulator into the semiconductor substrate;

removing the doped insulator from around the remainder portion of the first conductive layer;

forming a dielectric layer on the walls of the trench in the remainder portion of the first conductive layer; and

forming a second conductive layer within the trench, on the dielectric layer.